ONE GIGABIT/SECOND SIGNAL PROCESSING AND DATA HANDLING

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Abstract

An overview of hardware developments allowing digital communication and data handling at a 1-Gb/s rate is presented. The signal processing hardware includes a 1-Gb/s QPSK modem, 500-Mb/s bit synchronizer – signal conditioners, and a test system. The data handling equipment includes developments for multiplexing, demultiplexing, recording, and analog-to-digital conversion. The signal plus noise performance of the modem and the bit synchronizer – signal conditioner is discussed.

Introduction

The multiplexing of many sources and/or the analog-to-digital conversion of wideband sources has led to high bit rate requirements for digital communication networks. Requirements for rates as high as 1 Gb/s have already been identified. In the past, Radiation has developed hardware operating near theoretical at data rates to 400 Mb/s[1][2][3]. The extension of this capability to 1 Gb/s is discussed in this paper. QPSK, quadraphase shift keying, was chosen as the modulation format for its efficiency and bandwidth requirements. The hardware was developed for use over both microwave and optical links. In a microwave system the QPSK microwave subcarrier is upconverted to the microwave carrier frequency. In the optical link, the QPSK microwave subcarrier modulates the optical carrier. Optical demodulation after transmission generates the QPSK microwave subcarrier. Demodulation and detection at this point is then common for both systems. The noise is Gaussian in the first case and mixed Gaussian – Poisson in the second case. Once an estimate of the data state for each bit period has been made, then the remaining processing or data handling is digital in nature and independent of the type of link.

Summary

A block diagram of the QPSK modem is presented in Figure 1. Two quadrature 1.5-GHz carriers are biphase modulated at a 500-Mb/s rate and combined to generate a 1-Gb/s QPSK signal. The modulator also has test hardware in its enclosure to add broadband bandpass noise and any desired filtering for laboratory link simulation and performance testing. The bandwidth of the modulator exceeds 2 GHz.

As shown, the noise-corrupted QPSK input to the demodulator is power split into two paths. In one path S+N is bandpass filtered and routed to an X4 nonlinearity whose output has an unmodulated carrier at 6 GHz. This is bandpass filtered and is used as the reference input to a phase-lock loop. The loop has a phase-coherent 1.5-GHz output that is split into quadrature components which are the reference inputs for the demodulation phase detectors. In the other path, S+N is routed to the phase detectors. The IF outputs of the phase detectors are the two original 500-Mb/s bit streams corrupted by noise. The throughput bandwidth of the demodulator also exceeds 2 GHz.

The Bit Synchronizer – Signal Conditioner (BSSC) block diagram is presented in Figure 2. One purpose of this unit is to optimally filter and make data state estimates at the end of each bit period. In addition, a bit rate phase-coherent clock is generated to control the decision process and to provide a clock for following hardware. As shown, the baseband S+N is first filtered in a time-invariant low-pass filter whose impulse closely matches that of the sliding integral. The output y(t) is then routed into two paths. In the timing path y(t) is full wave rectified. At this point, a bit rate spectral component has been generated which is then bandpass filtered for signal-to-noise enhancement, and for memory since transitions are not always present. The bandpass filter output is the reference input to a phase-lock loop that provides further signal-to-noise improvement and memory. The buffered VCO output of the loop is an overall output that is also routed to the decision unit.

In the decision unit a narrow pulse is generated at the end of each bit period if $y(t) > \Sigma$, a reference level. If $y(t) < \Sigma$, no pulse is generated. These pulses are processed to control logic circuitry that holds and converts the data state decisions to emitter-coupled logic levels. A 1:2 demultiplexer is part of the decision unit so that the output of the BSSC is two 250-Mb/s ECL bit streams. This feature was provided for convenience in testing and to allow interfacing with standard ECL.

A test set generates a $(2^{12} - 2)$ data pattern for performance testing. For BSSC testing, baseband noise is added to the bipolar bit stream and routed to the BSSC. The output of the BSSC is compared to the original pattern in the test system and errors detected. The number of errors divided by 50 is an output of the test system. For combined modem – BSSC performance testing, the noise-free 500-Mb/s PCM output of the tester is power split and routed with different delays to the two 500-Mb/s inputs of the QPSK modulators. The difference in these delays eliminates correlation between adjacent bits. Bandpass noise is added to the QPSK modulator output and the sum is routed to the demodulator. The demodulator outputs go the BSSC's. One of the BSSC data outputs is connected to the test system and bit errors are measured, as before.

Figure 3 is a photograph showing the BSSC, the QPSK modulator plus RF link simulator, the QPSK demodulator, and the test system. The performance of this hardware is presented in Figure 4. Over a 0- to 12-dB E_b/N_0 range the BSSC performance is within 1.2 dB of the non-bandlimited PSK theoretical curve. Over the same range, combined BSSC – modem performance is within 2.2 dB of theoretical. Performance over a 1-Gb/s optical link will also be discussed.

At the present time Radiation Systems Division is developing a digital data recorder that uses holographic techniques. With this concept data with rates approaching 1 Gb/s may be recorded. Hardware that multiplexes to 1 Gb/s and demultiplexes from 1 Gb/s is shown in Figure 5. This hardware, which is part of the wideband recorder development, has internal test circuitry which proves that the multiplexing – demultiplexing is error free.

Other related subjects to be discussed include analog-to-digital conversion, group synchronization, and decommutation for high data rates, as well as high-speed, low-power logic developments.

Conclusion

An overview has been presented of hardware developments that demonstrate that the signal processing and data handling required for 1-Gb/s digital communication is feasible, and that performance close to theoretical can be achieved.

References

1. J. S. Gray, "Signal Conditioning, Bit Synchronization and Group Synchronization for High Bit Rate PCM," National Telemetry Conference, Washington, D.C., April 1969.

2. J. S. Gray, "Considerations for High Bit Rate PCM," Proc. of the Sixteenth ISA Aerospace Instrumentation Symposiums, Seattle, Washington, May 11–13, 1970.

3. J. S. Gray, "Processing of NRZ PCM from 10 Mb/sec to 200 Mb/sec, "International Telemetry Conference, Los Angeles, California, October 1970.

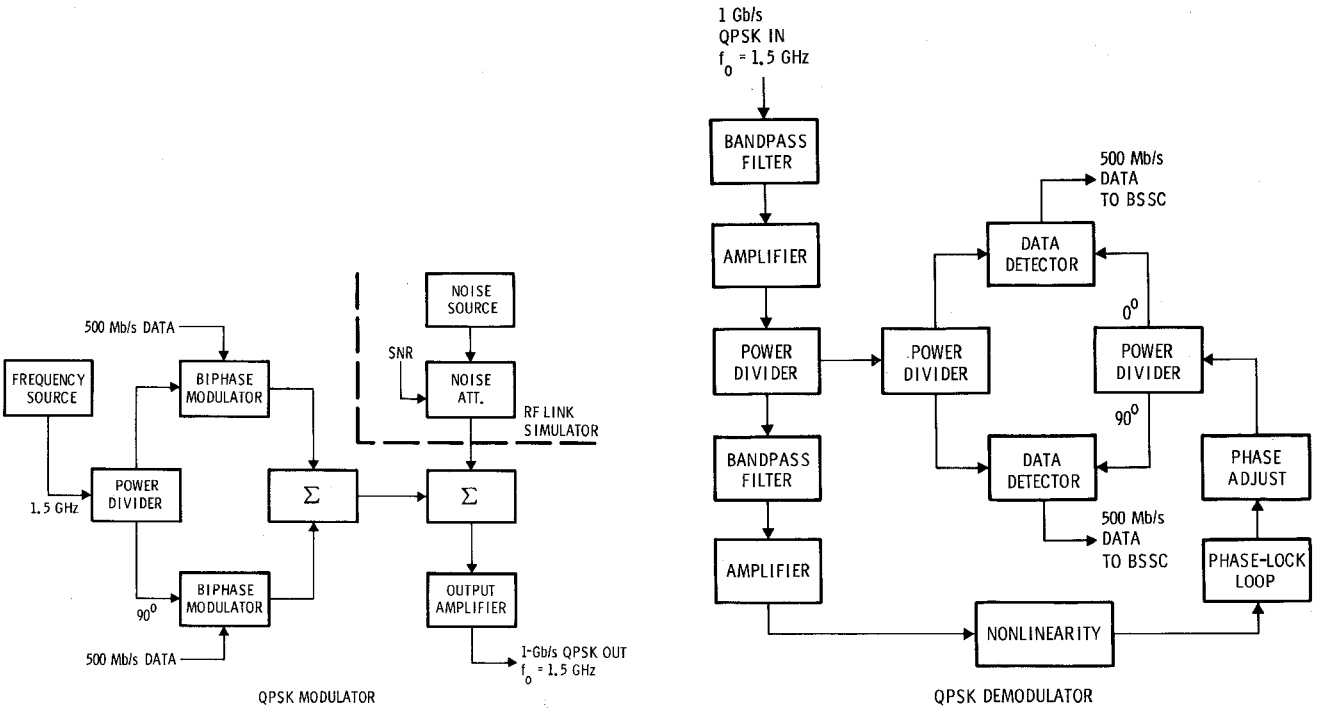

FIG. 1 1 Gb/s QPSK MODEM

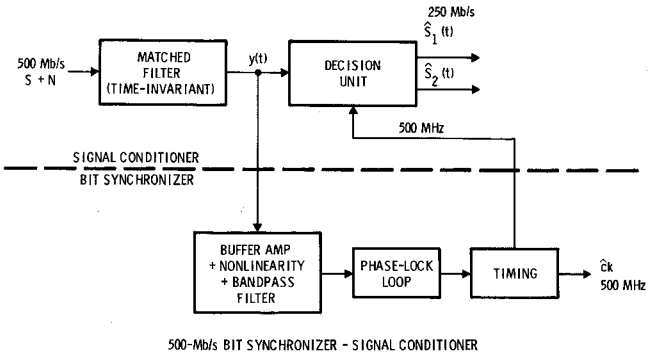

FIG. 2 500 Mb/s BIT SYNCHRONIZER - SIGNAL CONDITIONER (BSSC)

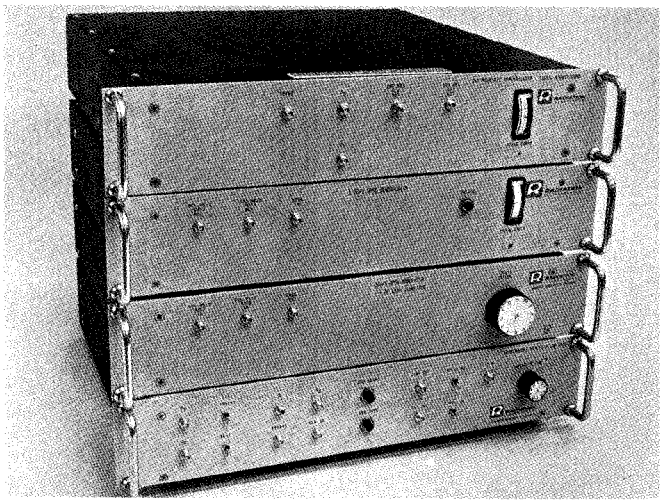

FIG. 3 500 Mb/s BSSC, 1 Gb/s QPSK MODULATOR + RF LINK SUMULATOR, 1 Gb/s QPSK DEMODULATOR, AND PERFORMANCE VERIFICATION UNIT

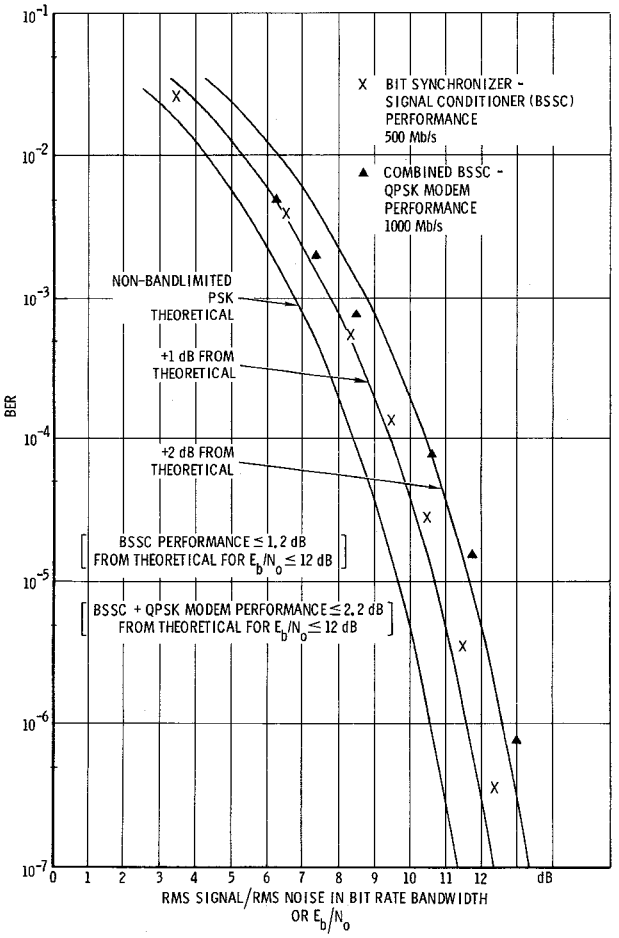

FIG. 4 SYSTEM PERFORMANCE

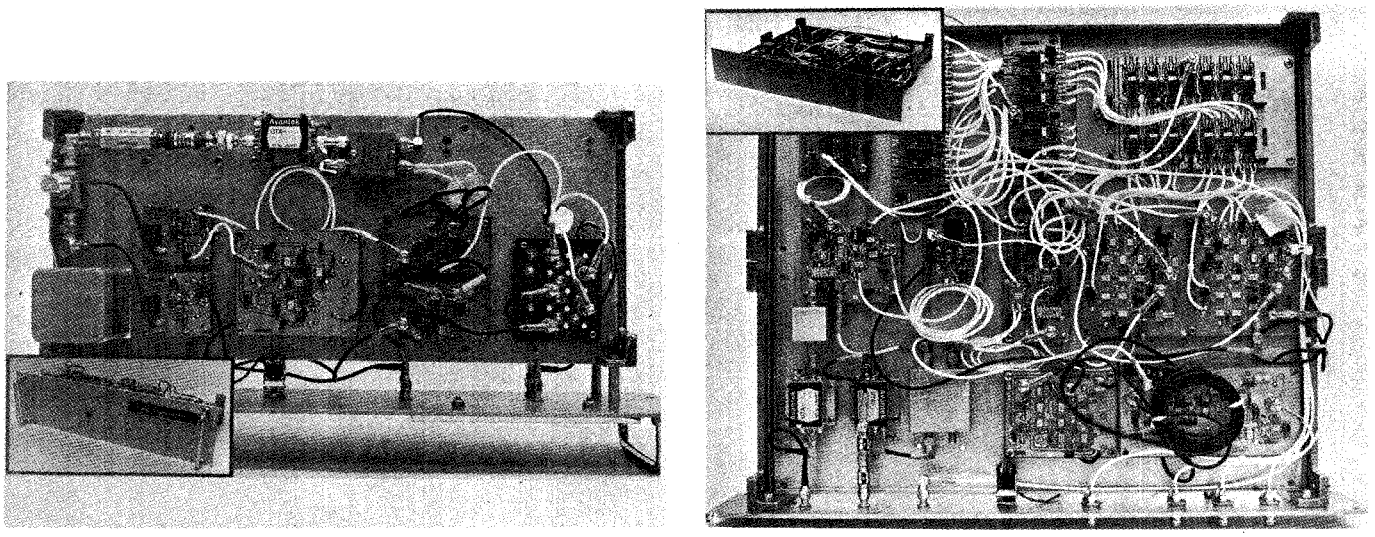

FIG. 5 1 Gb/s MULTIPLEXING - DEMULTIPLEXING HARDWARE